

Form PTO-1449 U.S. Department of Commerce (Rev. 8-88) Patent and Trademark Office		Attorney Docket No.: 0321.68261	Serial No.: 10/670,134
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Applicant: Andrew B. Kahng	
		Filing Date: 9/24/2003	Group: 3661 2826

MAR 08 2004
U.S. PATENT & TRADEMARK OFFICE

NL	Albrecht, "Global Routing by New Approximation Algorithms for Multicommodity Flow", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 20(5), May 2001, pp. 622-632.
AV	Alpert et al., "A practical methodology for early buffer and wire resource allocation", Proc. DAC, 2001, pp. 189-194.
✓	Alpert et al., "A practical methodology for early buffer and wire resource allocation", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22(5), 2003, pp. 573-583.
✓	Alpert et al., "Minimum buffered routing with bounded capacitive load for slew rate and reliability control", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 3, March 2003, pp. 241-253.
✓	Alpert et al., "Is wire tapering worthwhile?", Proc. ICCAD, 1999, pp. 430-435.
✓	Carden et al., "A global router using an efficient approximate multicommodity multiterminal flow algorithm", Proc. DAC, 1991, pp. 316-321.
✓	Carden et al., "A Global Router with a Theoretical Bound on the Optimum Solution", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 1996, pp. 208-216.
✓	Chen et al., "The Berkeley building-block (BBL) layout system for VLSI design", VLSI 83, Proceedings of the IFIP TC WG 10.5 International Conference on Very Large Scale Integration, Trondheim, Aug. 1983, pp. 37-44.
✓	Chen et al., "BBL: A Building Block Layout System for Custom Chip Design", Proc. IEEE Int. Conf. on Computer-Aided Design, Sept. 1983, pp. 40-41.
✓	Cong et al., "Performance optimization of VLSI interconnect layout", Integration 21 (1996), pp. 1-94.
	Cong, "Pin Assignment with Global Routing for General Cell Design," IEEE Trans. on CAD 10(11) (1991), pp. 1401-1412.
	Cong, et al., "Buffer block planning for interconnect-driven floorplanning", Proc. ICCAD, 1999, pp. 358-363.
	Dai et al., "Simultaneous floor planning and global routing for hierarchical building-block layout", IEEE Trans. on CAD 6(5) (1987), pp. 828-837.
	Dragan et al., "Practical approximation algorithms for separable packing linear programs", Proc. 7th Workshop on Algorithms and Datastructures (WADS), 2001, pp. 325-337.
	Dragan et al., "Provably good global buffering by generalized multiterminal multicommodity flow approximation", IEEE Transactions on Computer-Aided Design, 21(3), March 2002, pp. 263-274.
	Dragan et al., "Provably good global buffering by multiterminal multicommodity flow approximation", Proc. ASP-DAC, 2001, pp. 120-125.
✓	Dragan et al., "Provably good global buffering using an available buffer block plan", Proc. ICCAD, 2000, pp. 104-109.
NL	Fleischer, "Approximating fractional multicommodity flow independent of the number of commodities", SIAM J. Discrete Math., 13(4), (2000), pp. 505-520.
1	

Examiner Nan	Date Considered 08/05/05
-----------------	-----------------------------

*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 U.S. Department of Commerce (Rev. 8-88) Patent and Trademark Office		Attorney Docket No.: 0321.68261	Serial No.: 10/670,134
INFORMATION DISCLOSURE CITATION (Use several sheets if necessary)		Applicant: Andrew B. Kahng	
		Filing Date: 9/24/2003	Group: 3661 2828
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)			
NL	Garg et al., "Faster and simpler algorithms for multicommodity flow and other fractional packing problems", Proc. 39th Annual Symposium on Foundations of Computer Science, 1998, pp. 1-10.		
NL	Phillips, "The network inhibition problem", Proc. 25th Annual ACM Symposium on Theory of Computing, 1993, pp. 776-785.		
NL	Raghavan et al., "Randomized rounding: a technique for provably good algorithms and algorithmic proofs", Combinatorica, 7 (1987), pp. 365-374.		
NL	Tang et al., "Planning buffer locations by network flows", Proc. ISPD, 2000, pp. 180-185.		
Examiner	Name <i>Sam Lee</i>		Date Considered <i>07/06/05</i>
*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			